TEI INC.
SPECIAL SYSTEMS GROUP
HOUSTON, TEXAS

MCS
MICROCOMPUTER SYSTEM

SECTION V

TEI, INC. I/O 3P + 3S

PC BOARD

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P/N 13686-5

SECTION V

MCS-I/O 3P + 3S

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TEI, INC. 3P+3S I/O CARD

BASIC DESCRIPTION OF INPUT/OUTPUT

THIS CARD CONTAINS 3 SERIAL PORTS FOR INPUT & OUTPUT. TWO ARE ASYNCHRONOUS AND ONE PROGRAMMABLE AS SYNCHRONOUS OR ASYNCHRONOUS. IN ADDITION 24 BITS OF PARALLEL I/O ARE AVAILABLE.

UART (A): (AY 5-1013 U-10)
THIS SERIAL PORT COMES FACTORY SET TO PORT FF (HEX)-DATA
FE (HEX)-STATUS

8 CHARACTER BITS
2 STOP BITS (SYSTEM USE--FUNCTION KEYS AND BIT LIGHTS ON KEYBOARD)
EVEN PARITY

PORT ADDRESSING MAY BE CHANGED BETWEEN F8(HEX) THRU FF(HEX)
THE NUMBER OF CHARACTER BITS/STOP BITS/AND PARITY IS JUMPER OPTIONAL ALSO.

UART (B): (AY 5-1013 U-17)
THIS SERIAL PORT COMES FACTORY SET TO PORT 01(HEX)-DATA
00(HEX)-STATUS

7 CHARACTER BITS
2 STOP BITS (SYSTEM USE--KEYBOARD AND READY/BUSY LIGHTS)
EVEN PARITY

UART PORT ADDRESSING MAY BE CHANGED WITHIN 1 OF 16 PORTS SHARED BY 2 OTHER CHIPS (THE USART AND 8255A). THE 16 PORT BLOCK MAY BE MOVED WITHIN ANY 16 PORT BLOCK OUT OF THE 256 I/O PORT ADDRESSES. THE NUMBER OF CHARACTER BITS , STOP BITS , AND ODD OR EVEN PARITY ARE JUMPER SELECTABLE.

USART : (8251 U-3)
THIS IS A PROGRAMMABLE SERIAL INPUT/OUTPUT DEVICE

THIS SERIAL PORT COMES FACTORY SET TO PORT 02(HEX)-DATA
03(HEX)-STATUS

CHARACTER BITS, STOP BITS, PARITY, (SYSTEM USE--PRIMARILY ASSIGNED AS OPTIONAL RS 232 I/O FOR SERIAL PRINTER) AND OTHER FUNCTIONS ARE SOFTWARE PROGRAMMABLE.

.....

ALL 3 OF THE ABOVE SERIAL DEVICES HAVE TTL AND RS-232 DATA SIGNAL LEVELS FOR INTERFACING AVAILABLE AT THE I/O CARD CONNECTOR. ALL OTHER SERIAL (HANDSHAKING) SIGNAL'S ARE TTL ONLY.

.....

PARALLEL DEVICE: (8255A U-4)

THE 24 BIT I/O DEVICE OCCUPIES 4 PORT ADDRESSES AND COMES FACTORY SET TO THE FOLLOWING PORTS:

8255	PORT A	04(HEX) DATA
	PORT B	05(HEX) SYSTEM USE--PARALLEL PRINTER OUTPUT)
	PORT C	06(HEX) HAND SHAKING (STROBE, BUSY ...)
		07(HEX) COMMAND/CONTROL

* REFER TO 8255A DATA SHEET FOR DETAILS OF OPERATION.

THIS CARD IS DESIGNED TO OPERATE WITH A 2Mhz CLOCK PROVIDED FROM THE S100 BUSS. BAUD RATES ARE JUMPER SELECTABLE FOR 75 THRU 19,200 BAUD.

TO OPTION THE I/O CARD FOR SPECIAL PURPOSES, REFER TO I/O CARD OPTION TABLE.

****

DEVICE NO.	CHIP	TYPE	LOGIC FUNCTION
U1	9616	RS-232	DRIVER INTERNAL SLEW RATE LIMITING MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS SUPPLY INDEPENDENT OUTPUT SWING OUTPUT CURRENT LIMITING
U2	9617	RS-232	RECEIVER MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS FAIL-SAFE OPERATION INDIVIDUAL RESPONSE CONTROLS
U3	8251	USART	PROGRAMMABLE COMMUNICATION INTERFACE (SERIAL DATA) SYNCHRONOUS AND ASYNCHRONOUS OPERATION SYNCHRONOUS: 5-8 BIT CHARACTERS INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION AUTOMATIC SYNC INSERTION ASYNCHRONOUS: 5-8 BIT CHARACTERS PROGRAMMABLE CLOCK RATE-1, 16 or 64 TIMES BAUD RATE BREAK CHARACTER GENERATION 1, 1 1/2, OR 2 STOP BITS FALSE START BIT DETECTION FULL DUPLEX, DOUBLE BUFFERED, TRANSMITTER AND RECEIVER ERROR DETECTION--PARITY, OVERRUN, AND FRAMING
U4	8255A	PROGRAMMABLE PERIPHERAL INTERFACE	(PARALLEL - 3 EIGHT BIT PORTS) 24 PROGRAMMABLE I/O PINS DIRECT BIT/RESET CAPABILITY INTERRUPT CONTROL CAPABILITY

U5, U11, U12, AND U18	7493	4-BIT BINARY COUNTER (BAUD RATE)
U6	7421	DUAL 4-INPUT AND GATE (PORT ADDRESSES DECODE CIRCUIT)
U7	7400	QUAD 2-INPUT NAND GATE (PORT ADDRESS DECODE CIRCUIT) (1/2 OF THIS CHIP IS UN-USED)
U8	74368	TRI-STATEABLE LINE DRIVER (DECODE AND UART STATUS)
U9	7402	QUAD 2-INPUT NOR GATE (UART/USART-READ/WRITE LOGIC)
U10	AY-5-1013A	UART (A) SYSTEM KEYBOARD
U13	74154	ONE OF SIXTEEN DECODER (PORT DECODE CHIP)
U14	7410	3-INPUT NAND GATE (READ/WRITE LOGIC
U15	7400	QUAD 2-INPUT NAND GATE (READ/WRITE LOGIC)
U16	74368	TRI-STATEABLE LINE DRIVER (READ/WRITE-UART STATUS)
U17	AY-5-1013A	UART (B) (SYSTEM KEYBOARD (8) BIT LIGHTS)
U19	7430	8-INPUT NAND GATE (PORT F8-FF(HEX) DECODE CIRCUIT)
U20	7404	HEX INVERTER (ADDRESS BIT INVERSION (PORT BITS))
U21	74138	ONE OF EIGHT DECODER (PORT F8-FF (HEX))
U22 & U23	8216	4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER (DATA BUFFERS INPUT/OUTPUT SYSTEM BUS

POWER REGULATION:

+5VDC POWER FOR TTL Vcc 2 7805 ON CARD REGULATORS WITH HEATSINK'S
+12VDC POWER FOR 9616 RS-232 DRIVER (ONLY +12VDC REQUIRED) ZENER DIODE IN759A
-12VDC POWER FOR UARTS, AND 9616 RS-232 DRIVER ZENER DIODE IN759A

SERIAL PORTS:

CONNECTOR J3 (34 PIN RIBBON CABLE) SIGNALS ARE AS FOLLOWS

PIN #	FUNCTION
1	UART B XMIT (TTL)
2	UART B RECV (TTL)
3	UART B XMIT (RS-232-C)
4	UART B RECV (RS-232-C)
5	SYSTEM HARDWARE RESET FROM KEYBOARD
6	EXT CLR SYSTEM KEYBOARD SIGNAL (NEG. TRUE)
7	UART CLOCK (CAN RECEIVE OR TRANSMIT CLOCK)
8	+8VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
9	+16VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
10	-16VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
11	GROUND (POWER AND SIGNALS)
12	UART A XMIT (TTL)
13	UART A RECV (TTL)
14	UART A XMIT (RS-232-C)
15	UART A RECV (RS-232-C)
16	GROUND (SIGNAL)
17	+8VDC UN-REGULATED RAW POWER
18	+16VDC UN-REGULATED RAW POWER
19	-16VDC UN-REGULATED RAW POWER
20	GROUND (POWER)
21	SNYC DET. OUTPUT (USART SIGNAL (SYNCHRONOUS MODE))
22	RECIEVER READY (USART)
23	XMIT EMPTY (USART)
24	DATA TERMINAL READY (USART) (NEG. TRUE)
25	CLEAR TO SEND (USART) (NEG. TRUE)
26	DATA SET READY (USART) (NEG. TRUE)
27	REQUEST TO SEND (USART) (NEG. TRUE)
28	DATA TERMINAL READY (USART) (NEG. TRUE)
29	USART CLOCK (BAUD RATE CLOCK GEN.) (CAN RECEIVE OR TRANSMIT CLOCK)
30	GROUND (SIGNAL)
31	USART XMIT (RS-232-C)
32	USART RECV (RS-232-C)
33	USART XMIT (TTL)
34	USART RECV (TTL)

NOTE: JUMPERS "VS" MUST BE JUMPERED TO +8, +16, AND -16 TO HAVE POWER (RAW) EXIT THROUGH CABLE J3 THESE JUMPERS ARE TO KEEP RAW D. C. POWER OUT OF CABLE IF NOT NEEDED. THESE 3 JUMPERS ARE SHIPPED CONNECTED FOR KEYBOARD POWER. SINCE POWER IS AVAILABLE AT THIS CONNECTOR, EXTREME CAUTION SHOULD BE USED IN WIRING UP CABLES TO THIS CONNECTOR. IF POWER IS NOT NEEDED FROM THIS SOURCE, CUT THE JUMPERS ON THE CARD TO REMOVE POWER FROM THE CONNECTOR. IF USED, THE POWER IS NOT FUSED ON THE CARD, AND ANY PROTECTION FROM OVERLOAD MUST BE INHERENT IN THE MOTHERBOARD POWER SOURCE AND/OR PRE-CAUTIONARY STEPS MUST BE APPLIED IN THE PERIPHERAL THAT USES THIS POWER. COMBINED CURRENT AVAILABLE FOR PERIPHERALS SHOULD NOT EXCEED THE FOLLOWING:

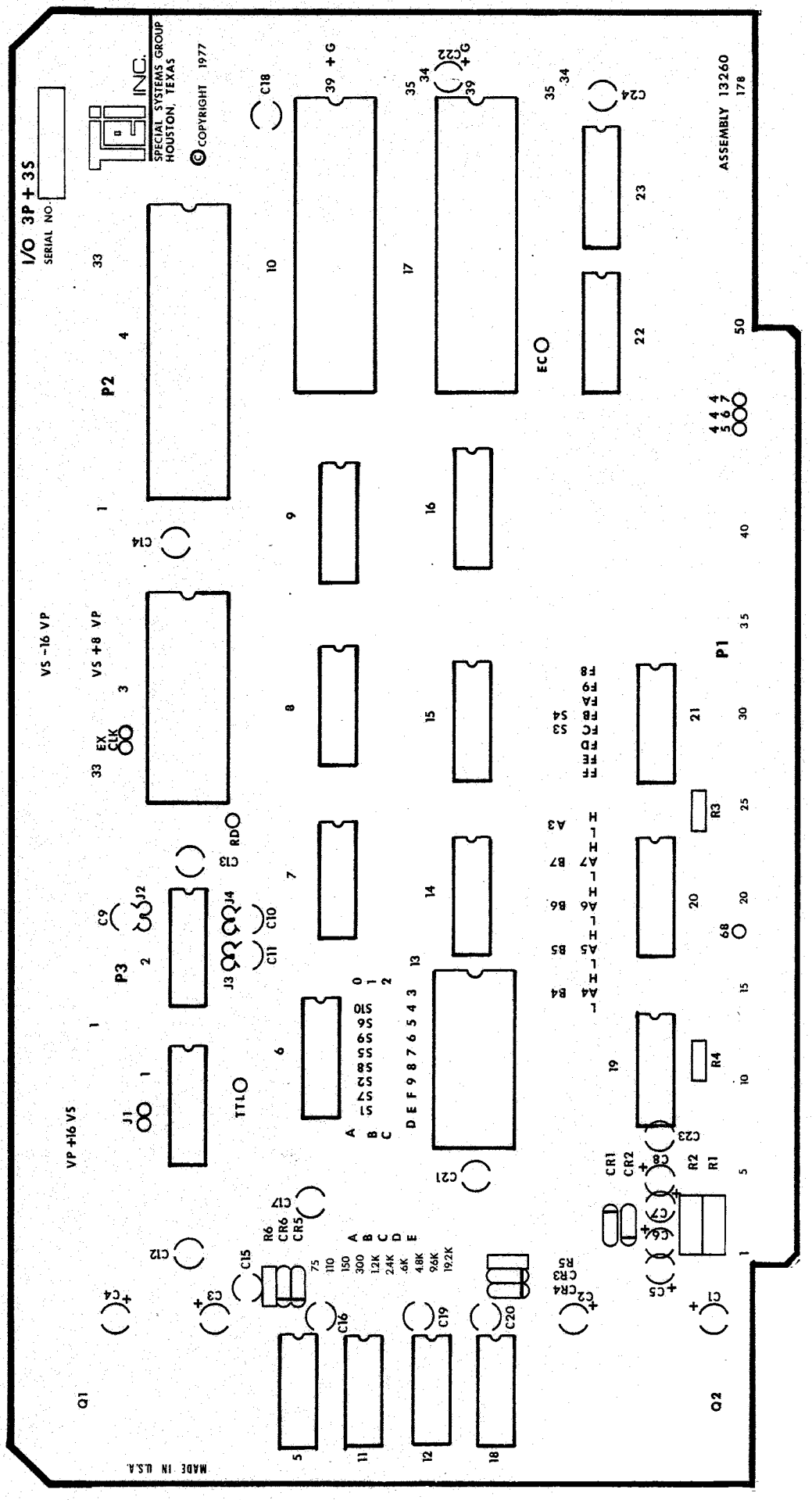
+8V	+16V	-16V
200MA	100MA	100MA

PARALLEL CABLE (CONNECTOR J2)

1	PORT B BIT 0
2	PORT B BIT 1
3	PORT B BIT 2
4	PORT B BIT 3
5	PORT B BIT 4
6	PORT B BIT 5
7	PORT B BIT 6
8	PORT B BIT 7
9	PORT C BIT 0
10	PORT C BIT 1
11	PORT C BIT 2
12	PORT C BIT 3
13	GROUND (SIGNAL)
14	+8 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
15	-16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
16	+16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
17	GROUND (POWER)
----------SPLIT CABLE HERE FOR CUAL 12 BIT PORT CONTROL----------	
18	+16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
19	-16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
20	+8 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
21	GROUND (POWER)
22	PORT C BIT 4
23	PORT C BIT 5
24	PORT C BIT 6
25	PORT C BIT 7
26	GROUND (SIGNAL)
27	PORT A BIT 0
28	PORT A BIT 1
29	PORT A BIT 2
30	PORT A BIT 3
31	PORT A BIT 4
32	PORT A BIT 5
33	PORT A BIT 6
34	PORT A BIT 7

NOTE: JUMPER "VP" MUST BE CONNECTED TO +8, +16, AND -16 IN ORDER TO MAKE POWER AVAILABLE AT CONNECTOR J2. ALL THE PRECAUTIONS COVERING RAW POWER FOR THE SERIAL CONNECTOR.

MCS- I/O 3P+3S COMPONENT LAYOUT



TEI INC.

PARTS LIST

MCS-3P+3S I/O Board

REF DES	DESCRIPTION	TEI P/N
C1, C2, C3, C4, C5, C6, C7, C8	Cap 10 uf @ 20V	1580-001
C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24	Cap, .1 uf	1562-002
CR1, CR2	Diode IN759A	4840-011
CR3, CR4, CR5, CR6	Diode IN916	4825-009
Q1, Q2	Regulator 7805	3120-003
R1	150 Ω 1/2 W 10% RES	4725-258
R2	120 Ω 1/2 W 10% RES *	4725-249
R3, R4, R5, R6	RES. 4.7K 1/4 W 2%	4741-402
U1	IC Chip 9616	3160-009
U2	IC Chip 9617	3160-010
U3	IC Chip 8251	3162-005
U4	IC Chip 8255	3162-006
U5, U11, U12, U18	IC Chip 7493	3161-012
U6	IC Chip 7421	3161-014
U8, U16	IC Chip 74368	3161-010
U9	IC Chip 7402	3161-019
U10, U17	IC Chip AY5-1013	3100-013
U13	IC Chip 74LS154	3164-008
U14	IC Chip 7410	3161-034
U15, U7	IC Chip 7400	3161-018
U19	IC Chip 7430	3161-032
U20	IC Chip 7404	3161-016
U21	IC Chip 74LS138	3164-009
U22, U23	IC Chip 8216	3162-002
P2, P3	Connector, 34 Pin	2125-012
-	Card Ejector	1700-001

* 100Ω may be used for R2.

REF DES	DESCRIPTION	TEI P/N

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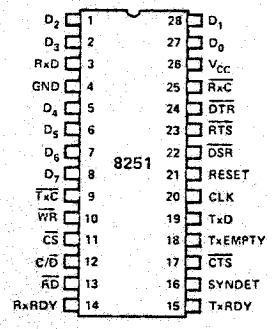
intel

8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1, 16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

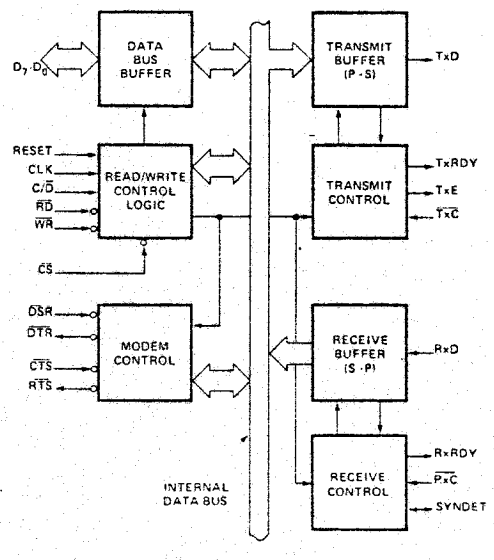
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



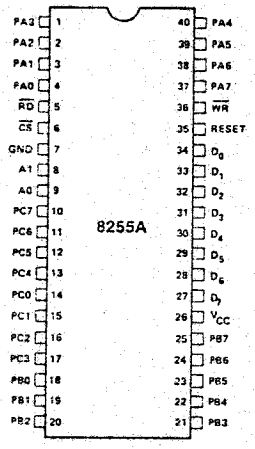
8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with MCS-80™ Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual-In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The 8255A is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

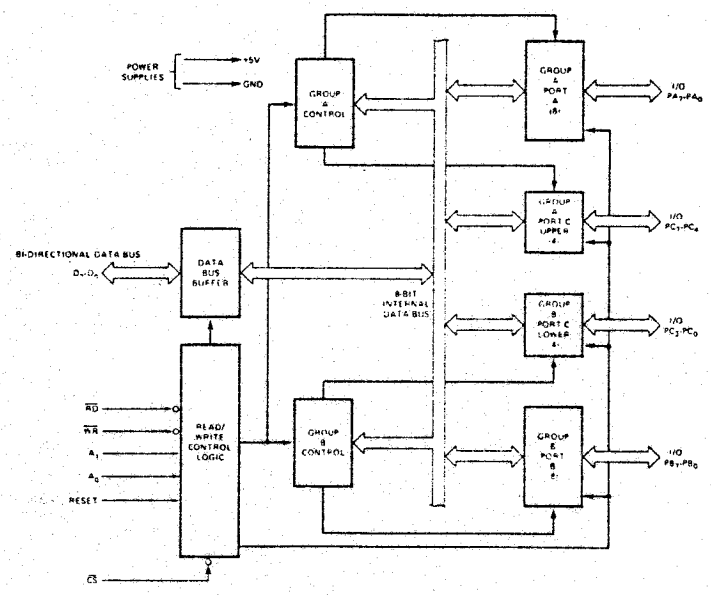
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM



UAR/T Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TLL compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- High Speed Operation.
- Three-State Outputs—bus structure capability.
- Low Power-minimum power requirements.
- Input Protected—eliminates handling problems.

AY-5-1013/1013A
- GIANT P-channel nitride process.
- 0 to 30kbaud/0 to 40kbaud.
- Pull up resistors to V_{CC} on all inputs.

AY-6-1013
- GIANT P-channel nitride process.
- 0 to 20kbaud.
- Extended Operating Temperature Range:
  -40°C to +85°C (plastic package)
  -55°C to +125°C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs.

AY-3-1014A/1015
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015)
- CMOS compatible (AY-3-1014A).
- 1½ stop bit mode.
- External reset of all registers.
- GIANT II N-channel Ion Implant Process.
- 0 to 30kbaud.
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015).

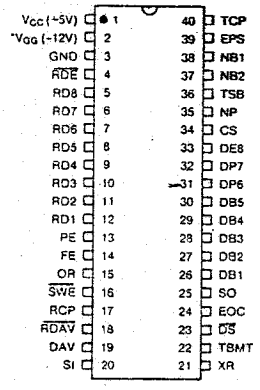
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN CONFIGURATION

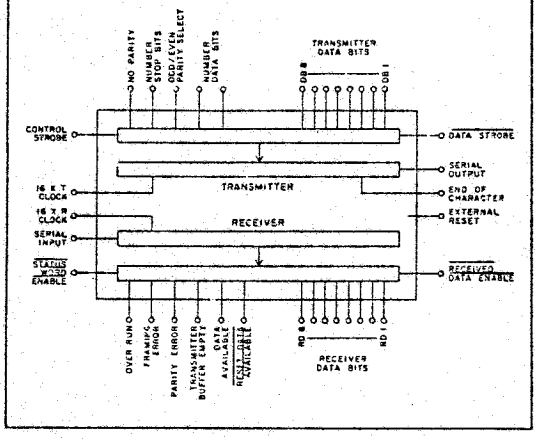
40 LEAD DUAL IN LINE

Top View



*Pin 2: AY-3-1014A/1015 — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	−12V Supply (Not connected for AY-3- 1014A/1015)
3	Ground (V_{GI})	Ground
4	Received Data Enable ($\overline{RDE}$)	A logic "O" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "O" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This lines goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable ($\overline{SWE}$)	A logic "O" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic "O" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "O") transition is required for initiation of data reception. Fig.11,12,33,34.
21	External Reset (XR)	Resets all registers (except that the received data register is not reset in the AY-5-1013/1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "O". Clears input data buffer. Must be tied to logic "O" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig.18,20,40,42.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig.17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig.16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "O".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "O" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TTL/MSI 9393/5493, 7493
4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input $\overline{CP}_B$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input $\overline{CP}_B$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

		LOADING
R_0	Reset-Zero Input	1 U.L.
$\overline{CP}_A$	Clock (Active LOW going edge) Input	2 U.L.
$\overline{CP}_B$	Clock (Active LOW going edge) Input	2 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

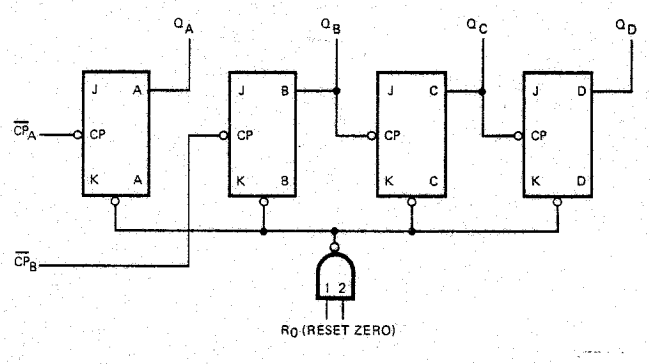
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE (See Notes 1, 2 and 3)

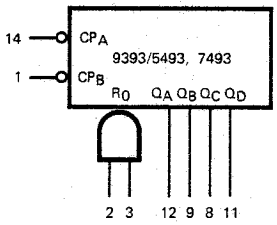
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES:
1. Output Q_A connected to input $\overline{CP}_B$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM

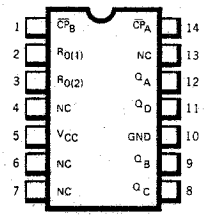


LOGIC SYMBOL

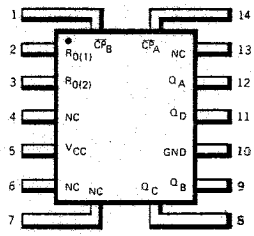


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No Internal Connection
Positive logic: See Truth Table

μA9616

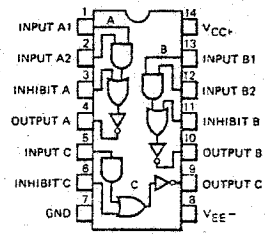
TRIPLE EIA RS-232-C LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24. Each driver in the μA9616 converts TTL/DTL logic level to EIA/CCITT levels for transmission between data terminal equipment and data communication equipment. The μA9617 performs the complementary functions. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH level on the inhibit terminal interrupts signal transfer and forces the output to a $-V_{OUT}$ or MARK state. The μA9616 is constructed on a single silicon chip using the Fairchild Planar* process.

- INTERNAL SLEW RATE LIMITING
- NO EXTERNAL CAPACITORS REQUIRED
- THREE CHANNELS PER PACKAGE
- MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS
- LOGICAL TRUE INHIBIT FUNCTION
- SUPPLY INDEPENDENT OUTPUT SWING
- OUTPUT CURRENT LIMITING

CONNECTION DIAGRAM
(TOP VIEW)



TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

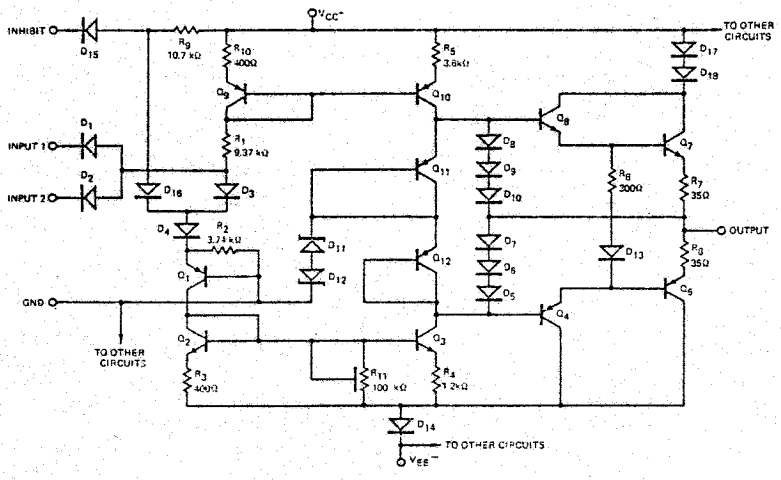
(For Channel C, omit INPUT 2 Column)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 to +6 V
Output Signal Voltage	±15 V
Maximum Power Dissipation (Note 1)	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1: Perate 8.3mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three channels)



*Planar is a patented Fairchild process.

μA9617

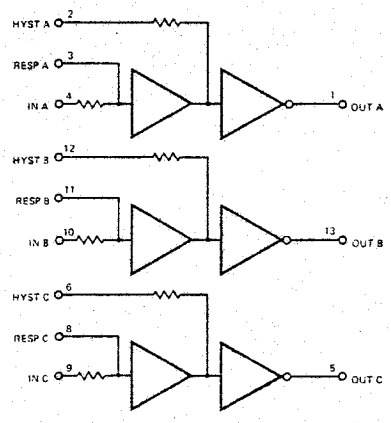
TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9617 is a Triple Line Receiver designed to meet the terminator electrical requirements of EIA RS-232-C AND CCITT V.24. It receives line signals produced by the μA9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground. The μA9617 is constructed on a single silicon chip using the Fairchild Planar* process.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

LOGIC DIAGRAM



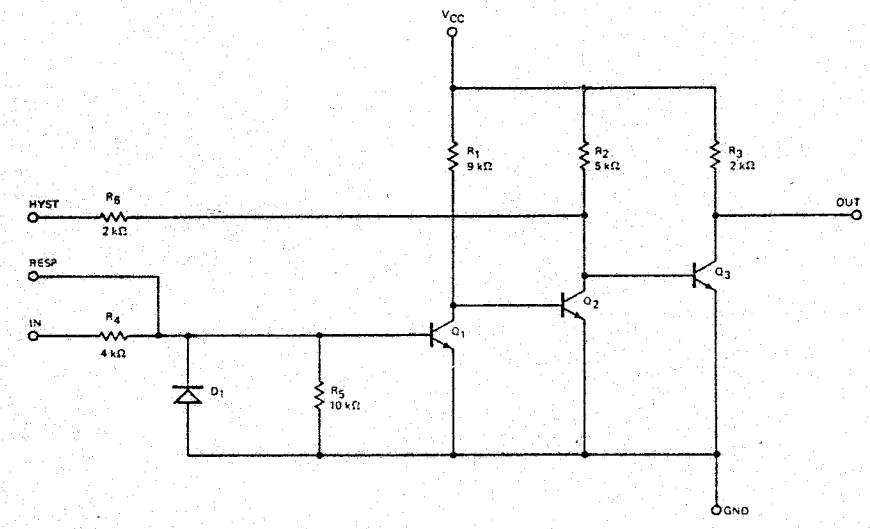
V_{CC} = Pin 14
GND = Pin 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25V
Output Current	25 mA
Maximum Power Dissipation (Note 1)	630mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1. Derate 8.3 mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

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